REMARKS

Claims 1-20 are all pending and all stand rejected under 35 USC §103(a). The references that have been cited against claims 1-20 include Tsai, Huang, Hobbs, and Gardener. Applicants have amended claims 1, 9, and 15. In view of the amendments and arguments set forth below, Applicants respectfully submit that all pending claims are now in condition for allowance.

35 USC §103(a) REJECTION OF CLAIMS 1-14

The Examiner has rejected claims 1-6 under 35 USC §103(a) as being unpatentable over Tsai in view of Huang and claims 7-14 under 35 USC §103(a) as being unpatentable over Tsai in view of Huang and Hobbs. Applicants have amended independent claims 1 and 9. Based on the amendment and the arguments below, Applicants respectfully traverse the Examiner's rejections.

According to MPEP §2143, "[t]o establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations". Applicants respectfully note that the Examiner has failed to establish any of the three criteria required by MPEP §2143. More specifically, there is absolutely no suggestion or motivation to combine Tsai and Huang, and there can be no reasonable expectation of success when they are combined. Finally and most importantly, the two references, even when combined, fail to teach all of the limitations of independent claims 1 and 9.

1. SUGGESTION OR MOTIVATION TO COMBINE

MPEP §2143 requires that there be "some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of

ordinary skill in the art, to modify the reference or to combine reference teachings." It is critical to note that claims 1-20 are directed to implementations of an invention that improves the deposition of spacers during a replacement gate process for 45nm transistors. When one of ordinary skill in the art is confronted with finding a method to improve spacer deposition on transistors this size, they will be motivated to look for art that deals with replacement gate processes and/or the deposition of spacers. Tsai and Huang, however, are completely off-topic and not relevant to replacement gate processes or deposition of spacers. Instead, Tsai addresses etching a metal silicide without removing too much polysilicon while Huang addresses the deposition of metal silicide. Accordingly, one of skill in the art would never look to Tsai or Huang when dealing with the issue addressed by the Applicants.

Furthermore, both Tsai and Huang actually teach away from the invention claimed by the Applicants. Both of these references teach the use of polysilicon and metal silicide (i.e., "polycide") in an interconnect and a metal gate electrode. The use of polysilicon and silicide in a metal gate electrode is an older technology that suffers from many problems. Contrary to this, claims 1-20 teach a newer method where a replacement metal gate process is used to form a metal gate electrode. The use of metal in the gate electrode is a substantial improvement over the older "polycide" approach. It is important to note that one of skill in the art, when looking for methods to improve spacer deposition in a replacement metal gate process, would never search for prior art that uses "polycide" in the gate electrode because the two technologies are very different and use completely different fabrication processes.

Additionally, Tsai further teaches away from claims 1-20 because Tsai requires the sidewalls of the trench be "at least about 88° with a plane of the substrate, and more preferable angles from about 89° to about 90°" (emphasis added, see col. 8, lines 16-18). Contrary to this, claims 1 and 9, as amended, recite that the sidewall meets "a plane of the dielectric layer at an angle that is less than about 87 degrees" (emphasis added). Tsai therefore teaches moving in

a direction that is opposite that of claims 1,9, and 15, and as such, Tsai clearly teaches away from what is claimed by the Applicants.

Accordingly, one of ordinary skill in the art would not be motivated to look to either of Tsai or Huang when searching for prior art to help address issues from a replacement gate process and from the deposition of spacers. Because of that, it is even less likely that one of ordinary skill in the art would ever be motivated to combine Tsai and Huang, as neither of these references deals with the problem addressed by the Applicants and neither reference contains language suggesting or motivating one to combine them.

Applicants note that the fact that both Tsai and Huang deal with the deposition of materials in an integrated circuit is not enough to provide a motivation to combine. There are literally hundreds if not thousands of patents and articles that deal with the deposition of materials in an integrated circuit. Here, it appears the Examiner has simply searched for unrelated patents that include some of the constituents of Applicants' claims 1-20 and then combined them to form a 103(a) rejection. However, as stated in MPEP 2141, "the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention." Here, Applicants believe that it is only with impermissible hindsight, based on a reading of the Applicants' claims, that one could be directed to combine the Tsai reference with the Huang reference. It is well established that this is not allowed. The Examiner has not provided any motivation to combine these particular references other than their both being from the same art. There needs to be something more to motivate one to seek out these specific references and then combine them to form the Applicants' invention.

2. REASONABLE EXPECTATION OF SUCCESS

When one of ordinary skill in the prior art is confronted with the task of improving the deposition of spacers during a replacement gate process for 45nm transistors, there is no reasonable expectation that simply combining the

teachings of Tsai and Huang will successfully produce the desired result. Again, MPEP 2141 states "the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention." This is because "the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure" *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)* (emphasis added). Furthermore, according to MPEP 2143.02, at least some degree of predictability is required. Accordingly, there must be something in Tsai and Huang that would give one of ordinary skill in the art the reasonable expectation that these references, when combined, would solve the issue of improving spacer deposition during a replacement gate process for 45nm transistors. Applicants note that Tsai and Huang do not provide even a minimal level of predictability.

As stated above, Tsai addresses etching a metal silicide without removing too much polysilicon while Huang addresses the deposition of metal silicide. One of ordinary skill in the art therefore would never look to Tsai or Huang and reasonably expect or predict that their methods of etching or depositing metal silicide would be even remotely applicable to spacer deposition during a replacement gate process. The Applicants cannot find anything in Tsai or Huang that would provide any reasonable expectation of success. Therefore, Applicants respectfully submit that the requirements of MPEP §2143 have not been met.

3. THE COMBINED REFERENCES FAIL TO TEACH ALL CLAIM LIMITATIONS

Finally and most importantly, Tsai and Huang, when combined, fail to teach all of the claim limitations. Claims 1 and 9, as amended, include the limitation "a sidewall meeting a plane of the dielectric layer at an angle that is less than about 87 degrees but sufficiently wide to enable a spacer to be formed on the sidewall...." This limitation is not taught or suggested by either Tsai or Huang. In fact, as noted above, Tsai teaches away from this limitation.

Rather than citing a prior art reference, the Examiner argues that "in a plasma etching environment the etch rate of the wet etch bath can be modified along with the duration of the etching process which will determine the width of the gate electrode. This would result in the width of the gate electrode varying depending upon the desired result. Therefore, one skilled in the art would readily recognize from the combination of Tsai and Huang would result a first width that is less than or equal to about 45 angstroms and the lower surface having a second width that is less than or equal to about 40 angstroms, wherein the first width is at least about 5 angstroms greater than the second width, since the variation in the first and second widths (i.e. more than 5 angstroms) would shorten the channel length that would increase operation speed of transistor." The Applicants respectfully note that this broad and general statement cannot be used to make claims 1 and 9 obvious.

This general statement by the Examiner does not provide enough guidance to one of ordinary skill in the art to find a solution to the issues that arise during spacer deposition in replacement metal gate processes. The fact that etching processes may cause variances in the sidewalls does not teach or suggest the intentional creation of a sidewall that meets a plane of the underlying dielectric layer at an angle that is less than 87 degrees. Allowing this general statement or observation made by the Examiner to make obvious a highly specific processing process, such as the intentional creation of an angled sidewall, sets a dangerous precedent that could stifle progress in the semiconductor processing arts.

Applicants stress that claims 1 and 9 recite the fabrication of a specific structure that has been found, through a significant amount of research and development, to improve spacer deposition in a replacement metal gate process. The Applicants respectfully assert that the Examiner's statement lacks the specificity needed to teach or suggest to one of skill in the art to etch the polysilicon layer to generate a sidewall that meets a plane of the underlying dielectric layer at an angle that is less than 87 degrees.

4. CONCLUSION REGARDING OBVIOUSNESS

Applicants urge the Examiner to consider the precedent that would be set in this art if claims are allowed to be rejected without an adequate showing of a motivation to combine, reasonable success, or teaching all of the claim limitations. If that becomes the case, then ANY potential layer deposition process that is developed for integrated circuit applications may be rejected on obvious grounds simply by using impermissible hindsight to find two references that disclose some of the claimed limitations, even if the newly formulated method consumed a tremendous amount of time and money to develop, and even if the new method produces results that are not yet known in the art, as is the case here.

Furthermore, the field of semiconductor processing is a crowded art in which there have been a large number of prior inventions. As the Examiner is aware, it takes less of an advancement to obtain a valid patent, otherwise one would have to conclude that there can be no further patenting in that art. The subtle differences between each of the articles and patents in this art, such as the specific process steps that are chosen, the specific sequence of those steps, the materials and dopants used in each layer, the types of etching processes that are performed, and the specific result that is sought after, are patentable distinctions that greatly affect the performance of the integrated circuit devices that are formed. As such, the advancements made by the Applicants, as recited in claims 1 and 9 are more than sufficient to merit patentability in this crowded art.

Based on the foregoing, Applicants submit that the Examiner has shown neither a reasonable expectation of success, a motivation to combine, nor a showing that all of the claim limitations can be found in the prior art when combined. Therefore, Applicants respectfully submit that the requirements of MPEP §2143 have not been met and, as such, believe that all of the elements of independent claims 1 and 9, as amended, are not made obvious by Tsai in view of Huang. Applicants therefore submit that the Examiner's rejection has been

overcome and that independent claims 1 and 9 are in condition for allowance, which is respectfully requested.

35 USC §103(a) REJECTION OF CLAIMS 15-20

The Examiner has rejected claims 15 and 17-20 under 35 USC §103(a) as being unpatentable over Hobbs in view of Gardener and Tsai and claim 16 under 35 USC §103(a) as being unpatentable over Hobbs, Gardener, and Tsai in view of Huang. Applicants have amended independent claim 15. Based on the amendment and the arguments below, Applicants respectfully traverse the Examiner's rejections.

Claim 15 has been amended to recite the claim limitation "...wherein a sidewall of the patterned polysilicon layer meets a plane of the patterned nitrided silicon dioxide layer at an angle that is less than about 87 degrees but sufficiently wide to enable a spacer to be formed on the sidewall...." This claim limitation, as described in the arguments above, has not been found in or made obvious by the prior art. Applicants therefore submit that the Examiner's rejection has been overcome and that independent claim 15 is in condition for allowance, which is respectfully requested.

PROVISIONAL OBVIOUS-TYPE DOUBLE PATENTING REJECTION OF CLAIMS 15-20

The Examiner has stated that claims 15-20 are provisionally rejected under an obvious-type double patenting rejection over claim 15 of copending application 10/739,173. The Applicants have amended claim 15 to recite the claim limitation "...wherein a sidewall of the patterned polysilicon layer meets a plane of the patterned nitrided silicon dioxide layer at an angle that is less than about 87 degrees but sufficiently wide to enable a spacer to be formed on the sidewall...." Accordingly, the Applicants believe that amended claim 15 is patentably distinct from claim 15 of copending application 10/739,173. As such, Applicants believe the obvious-type double patenting rejection has been overcome.

DEPENDENT CLAIMS

Applicants believe that the dependent claims are in condition at least by way of their dependence on an allowable base claim.

CONCLUSION

Applicant submits that all claims now pending are in condition for allowance. Applicant reserves the right to argue the patentability of the dependent claims. Such action is earnestly solicited at the earliest possible date. If there is a deficiency in fees, please charge our Deposit Account No. 02-2666.

Respectfully submitted,

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